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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/737,124	12/17/2003	Young-Doug Kim	8947-000074/US	5936

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EXAMINER	
DANG, KHANH	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 11/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/737,124	KIM ET AL.	
	Examiner	Art Unit	
	Khanh Dang	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

Claims 1-13, 29, and 30 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With regard to claims 1 and 2, it is unclear where the claimed limitation may begin and end. It is suggested that a transitional phrase such as "comprising", "consisting essentially of" or "consisting of" is used in the claims to define the scope of the claims.

With regard to claim 29, the step of "receiving" (line 1) lacks clear antecedent basis.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 19-33 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

At the outset, it is noted that the method recited in claims 19 and 26 is a computer program (see claims 25 and 33). The descriptions or expressions of the programs, are not physical "things." They are neither computer components nor statutory processes, as they are not "acts" being performed. Such claimed computer

programs do not define any structural and functional interrelationships between the computer program and other claimed elements of a computer which permit the computer program's functionality to be realized.

In order to overcome the 35 USC 101 rejection, independent claims 19 and 26 must be amended in such a way that they must be clearly directed to a method that is implemented by hardware. Applicants' own admission that these method claims can be performed using software or a computer program (see claims 25 and 33) may be used in light of 35 USC 101 against any method claim that does not include limitation in the claim that clearly indicates that the method is performed using hardware.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-10, 13-33 are rejected under 35 U.S.C. 102(b) as being anticipated by Kenny (6,393,506).

As broadly drafted, these claims do not define any structure that differs from Kenny.

With regard to claims 19-33, in order to expedite a complete examination of the instant application, claims 19-33 rejected under 35 USC 101 (nonstatutory) above are further rejected below in anticipation of applicant amending the claims to place them within the four statutory categories of invention.

With regard to claim 1, Kenny discloses an arbiter (arbiter 4, Fig. 1, for example) in a system (shown generally at Fig. 1) for generating a pseudo-grant signal to all requesting master units (the virtual channel grant signal is readable on the so-called "pseudo-grant signal." In particular, in Kenny, a master module initializes bus access by asserting address and bus request signals on the bus 11. The arbiter 4 and the slave module detect the address and request signals asserted by the master module. The arbiter 4 then identifies the master module making the request, determines the master module's priority, and grants a virtual channel. The virtual channel granted can be arbitrarily selected by an allocation procedure. Alternatively, each subsystem may be configured with a fixed virtual channel with a pre-assigned priority. Pre-designating virtual channels and priorities for each module simplifies processing by eliminating allocation procedures and requiring arbiter 4 to merely match the I/O address of the requesting master module to that master module's pre-assigned virtual channel and pre-assigned priority, referencing a table stored in a register of arbiter 4 or elsewhere. Upon detecting the master 's assertion of the ADD/REQ signal, the arbiter asserts signal GNT CHNLA to indicate assignment of a virtual channel to the master. After asserting signal GNT CHNLA, arbiter 4 returns to its initial state 47 to wait for the next ADD/REQ signal. A virtual channel is relinquished by the master module upon

completion of the data transfer for which the virtual channel was requested. The Arbiter 4 then removes the virtual channel from its list of granted virtual channels, thus allowing it to be reassigned to anther master/slave pair requesting data bus access. Alternatively, if a dynamic priority allocation scheme is used, the virtual channel's priority is reduced. Under one such scheme, the virtual channel is not taken away from its master and slave modules, unless a new virtual channel request is received by arbiter 4, and all virtual channels are granted) and for receiving transaction information from all requesting master units in response to the pseudo-grant signal (after asserting signal GNT CHNLA, arbiter 4 returns to its initial state 47 to wait for the next ADD/REQ signal from each of the master).

With regard to claim 2, it is clear that the arbiter 4 further performs arbitration based on the transaction information such as the pre-assigned priority received from the requesting master.

With regard to claim 3, it is clear that in Kenny, the arbiter 4 includes a master interface for interfacing with the masters (see at least Fig. 1 and description thereof) for generating the pseudo-grant signal (virtual channel grant signal GNT CHNLA) to all the requesting masters, for receiving the transaction information from all the requesting master units in response to the pseudo-grant signal (after asserting signal GNT CHNLA, arbiter 4 returns to its initial state 47 to wait for the next ADD/REQ signal from each of the master), and for generating a ready signal (CHNLA ACTIVE, for example) to a selected one of the requesting master units.

With regard to claim 4, it is clear that the arbiter 4's the master interface includes at least one generator for generating the pseudo-grant signals (GNT CHNLA) from at least one request signal (ADD/REQ) from all the requesting masters.

With regard to claim 5, it is clear that the master interface including at least one circuit for converting a target slave ready signal (CHNLA RDY) from at least one slave (also slave in Kenny) into a data transfer ready signal (CHNLA ACTIVE, for example) for a selected one of the requesting master units.

With regard to claim 6, it is clear that the ready signal (CHNLA RDY) is for data transfer.

With regard to 7, it is clear that data can only be transferred when the bus is available. In other words, the ready signal (CHNLA RDY) indeed indicates bus availability.

With regard to claim 8, it is clear that in Kenny, the arbiter including a controller interface for requesting at least one slave unit to prepare for data transfer in response to the target information (in Kenny, the target information is the address of the slave, ADD, for example) from the selected one of the requesting masters. Note that all modules as shown in Fig. 1, as in any conventional interconnected modules include respective interface for communication among modules. See also col. 5, line 28 to col. 6, line 21).

With regard to claim 9, it is clear that the controller interface is a slave controller interface which interacts with at least one slave controller of the at least one slave unit. Note that all modules as shown in Fig. 1, as in any conventional interconnected

modules) include respective interface for communication among modules. See also col. 5, line 28 to col. 6, line 21).

With regard to claim 10, it is clear that slave memory 6 includes slave controller to control the slave memory.

With regard to claim 13, each driver layer 12 of each master includes registers 21, 22 and 23. Registers 21, 22, and 23 latch read, address and write data, respectively. A master or system clock FCLK (not shown), is received at terminal 24 to synchronize registers 21, 22 and 23 with timing on the bus.

With regard to claims 14-33, see discussion above. With regard to claim 29, note also that it is clear from the discussion above that the steps of generating the request from a master, receiving the request and generating a virtual channel grant signal from the arbiter 4, supplying information from the master, and preparing for data transfer constitute a first stage and said completing and transferring constitute a second stage and said first and second stages occur concurrently.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kenny.

Kenny, as discussed above, discloses the claimed invention including the use of interface controllers for the arbiter and slave module such as the memory module 6. Kenny does not disclose the use of SDRAM (Synchronous Dynamic Random Access Memory). However, memory such as SRAM is old and well-known in the art as evidence by the definition of SDRAM provided by Wikipedia.com. cited below. SDRAM is an improvement to standard DRAM in that it retrieves data alternately between two sets of memory. This eliminates the delay caused when one bank of addresses is shut down while another is prepared for reading. It's called "Synchronous" DRAM because the memory is synchronized with the clock speed that the computer's CPU bus speed is optimized for. The faster the bus speed, the faster the SDRAM can be. In other words, SDRAM's timing is synchronized to the system clock. By running in sync to an external clock signal, SDRAM can run at the same speed as the CPU/memory bus. It would have been obvious to one of ordinary skill in the art at the time the invention was made to employ SRAM in memory module 6 of Kenny, since the use of SDRAM is old and well-known, as evidence by the definition of SDRAM provided by Wikipedia.com. cited below, for improving latency. Note also that since the interface controller of the arbiter 4 is in direct communication with the memory slave 6 SDRAM controller, it is clear that controller interface is an SDRAM controller interface which interacts with at least one SDRAM controller of the at least one slave unit.

U.S. Patent Nos. 6,671,761 to Kim, 6,857,035 TO Pritchard et al., 4,667,192 to Schmid, 5,935,234 to Arimilli et al., SDRAM Definition from Wikipedia, the Free Encyclopedia, and AMBA Specification, Rev. 2.0 are cited as relevant art.

Any inquiry concerning this communication should be directed to Khanh Dang at telephone number 571-272-3626.

Khanh Dang
Primary Examiner